PCB DFM GUIDELINES

By: O-Leading Process Engineering

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SECTION 1: INTRODUCTION

1.1 PURPOSE

This document is intended to be used as a guide in the engineering and layout of printed wiring boards and assemblies. Guidelines are presented to aid in the design of manufacturable and reliable printed wiring assemblies. PCB fabrication and assembly processes in common use are described along with the advantages and limitations concerning their application. Preferred processes and design practices are recommended to optimize the fabrication and assembly processes, as well as identify manufacturing limitations.

1.3 SCOPE

The guidelines and requirements in this document apply to the design and manufacture of printed wiring boards and assemblies. If possible, pad geometry and outer layers should be reviewed by qualified assembly personnel for potential problems. Proper pad design will allow the desired IR, vapor phase, convection, or wave solder results.

SECTION 2: GENERAL DESIGN STANDARDS

The following sections contain design standards common to printed wiring boards. In the case of small and flex type boards, where exceptions to these standards may be required, fabrication and assembly vendors should be consulted and approval sought from the responsible engineering group.

2.1 CIRCUIT LAYERS

All circuit layers, including power and ground layers, will contain the layer number etched in copper. The numbers will be staggered in such a way that all numbers, except for the bottom layer number, will be in order and readable when looking through the top of the board (see illustration below). The bottom layer number will be readable from the bottom of the board.

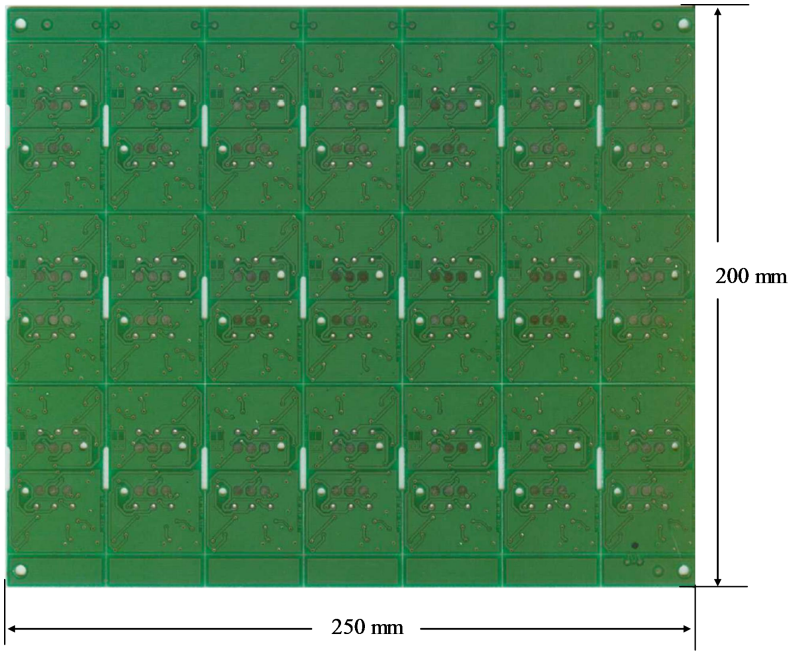
PLACING LAYER NUMBERS ON THE BOARD

2.2 SILKSCREEN AND COMPONENT ID

An attempt should be made to provide designators for all component outlines shown on the silkscreen. Designators should be readable when components are installed. Indicate pin 1 on all connectors, headers, crystals, and any other component where pin 1 is not readily identifiable.

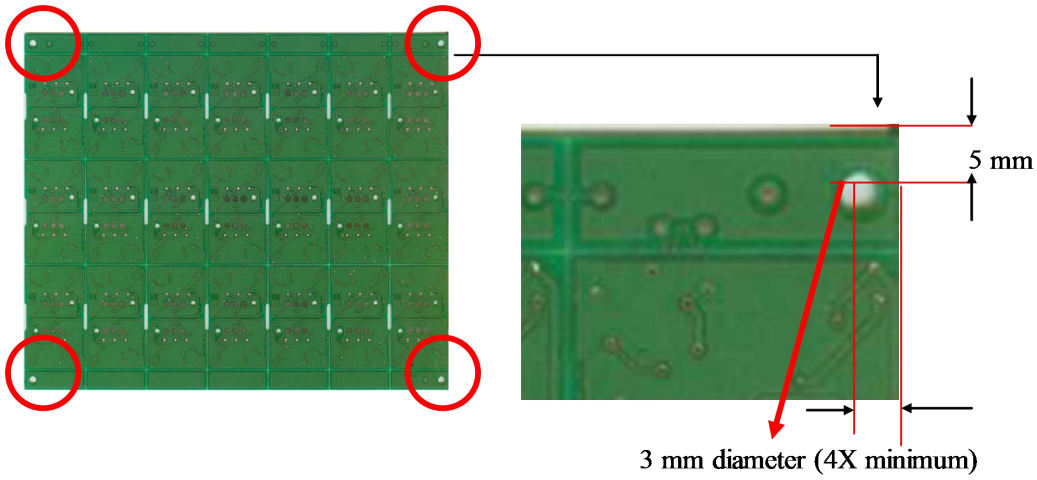
2.3 PANELIZATION

Recommended maximum panel dimension should not exceed 200 mm Width and 250 mm Length. Minimum panel dimension should not compromise the process performance and handling. Note: Panel dimension should also depend on PCB manufacturer panel sheet.



2.4 TOOLING HOLE

Recommended tooling hole diameter is 3 mm not plated.

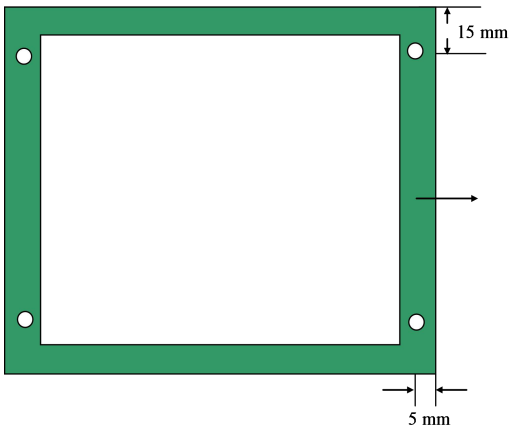


2.5 FIDUCIAL

2.5.1 Fiducial Location

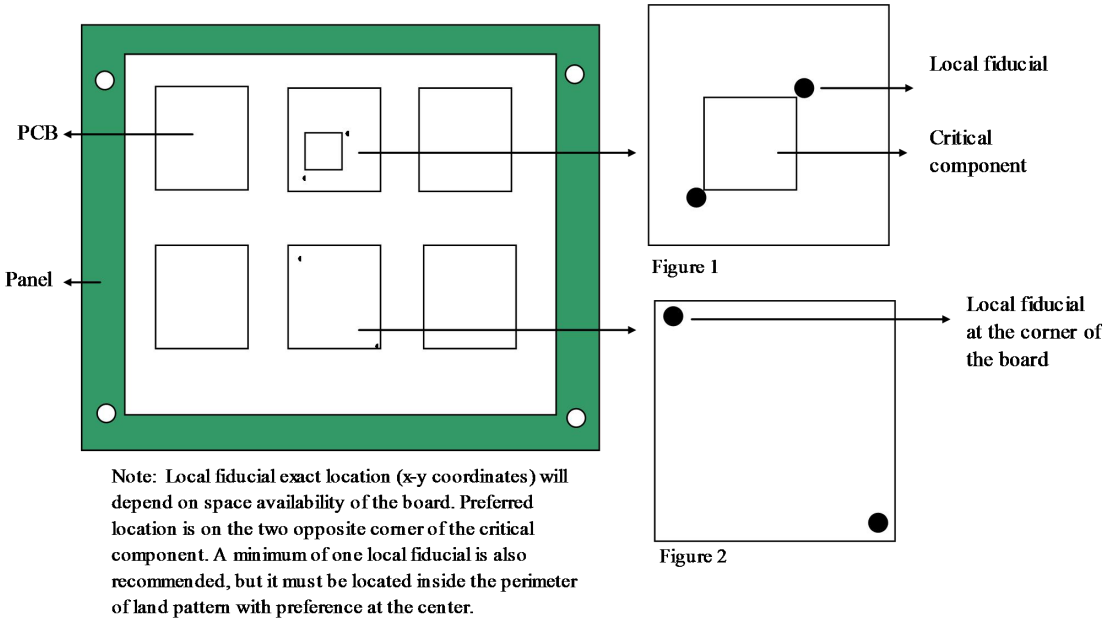
A. Global Fiducial

Fiducial location must be 15 mm from the edge Y-axis and 5 mm X-axis.



B. Local Fiducial

Fiducial location must be near to the critical components that needs high placement accuracy requirement (see figure 1). For very dense board that doesn't accommodate the fiducial near the critical component (BGA, flip chip, CSP, QFP), suggested location must be at the corner of the board (see figure 2).

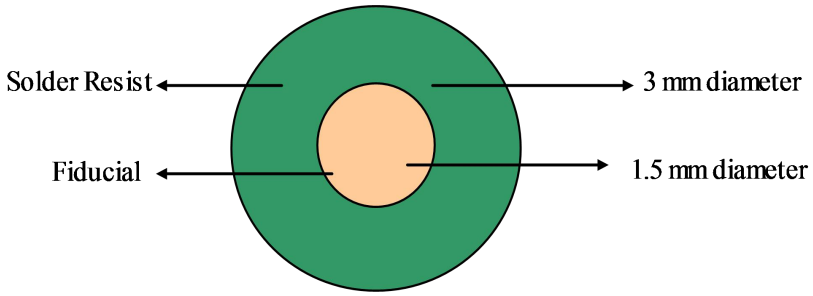


Note: Local fiducial exact location (x-y coordinates) will depend on space availability of the board. Preferred location is on the two opposite corner of the critical component. A minimum of one local fiducial is also recommended, but it must be located inside the perimeter of land pattern with preference at the center.

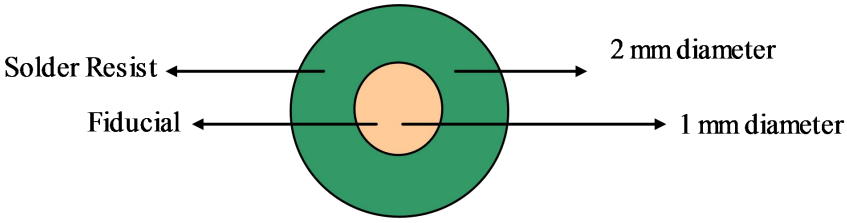
2.5.2 Fiducial Diameter

For panelized, multiple PCB's or boards with edge breakouts, fiducial can easily be positioned in the boarder, however, fiducials are still required on each individual circuit to maintain positional accuracy. Recommended fiducial diameter for global is 1.5 mm and 3.0 mm resist diameter and for local, 1.0 mm and 2.0 mm diameter respectively.

B.1 Global Fiducial



B.2 Local Fiducial



2.5.3 Fiducial Material

The following are the recommended material for fiducial:

1. Bare Copper
2. Bare Copper protected by a clear anti-oxidation coating
3. Nickel or Tin Plated or solder plated (Hot Air Levelled)

The preferred thickness of plating or solder coating is 0.005 mm to 0.010 mm {0.0002 to 0.0004 in.), should never exceed 0.025 mm [0.001].

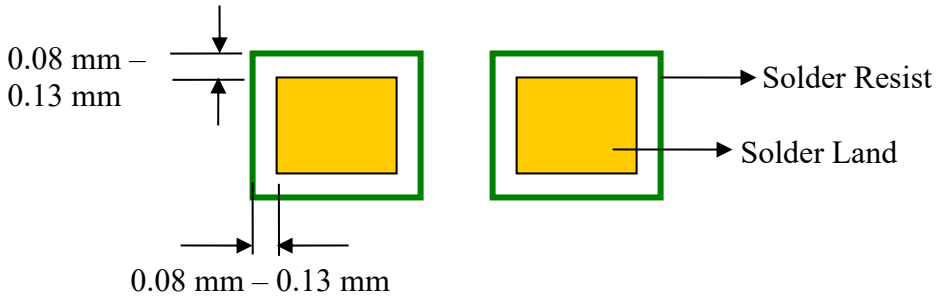
Note:

If solder mask is used, it should not cover the fiducial or the clearance area. It should be noted that oxidation of a fiducial mark's surface may degrade its reliability.

2.6 SOLDER RESIST

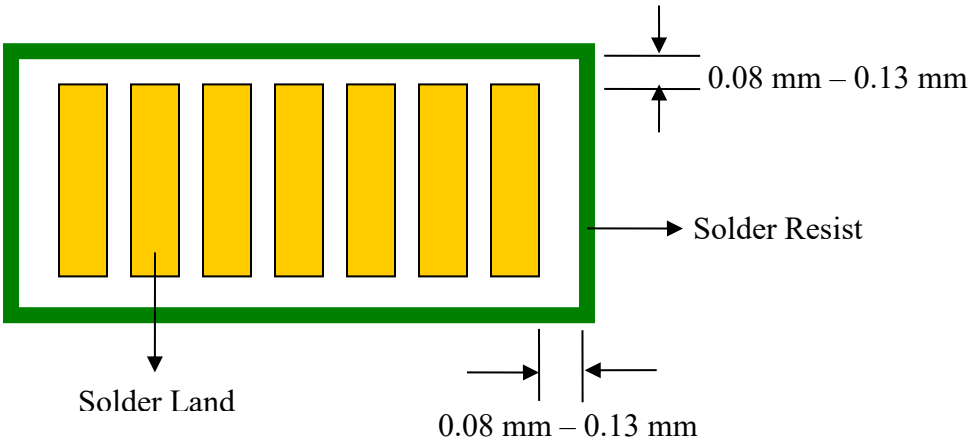
2.6.1 Non-Fine Pitch Pads

A clearance around solder pads should be 0.08 mm – 0.13 mm.



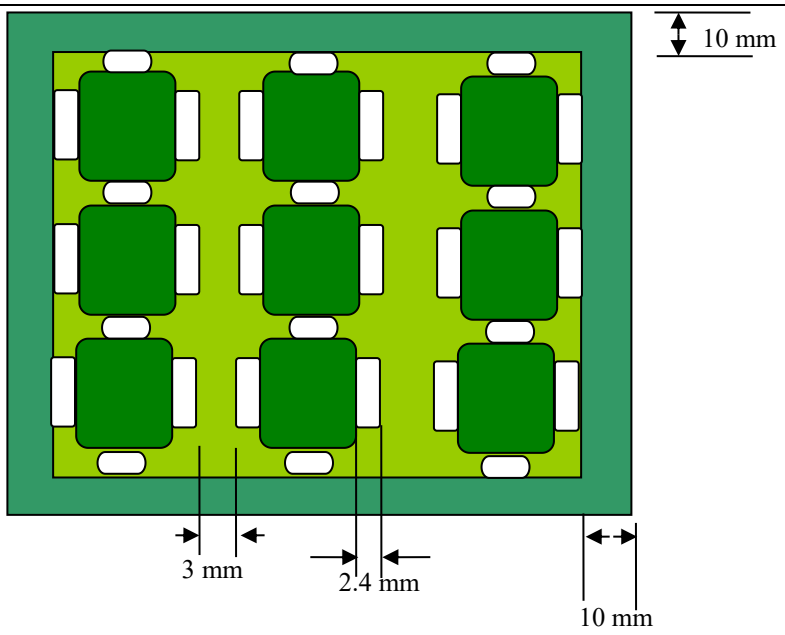
2.6.2 Fine Pitch Pads

On fine pitch pads (0.5mm and below), it may not be possible to put resist between the individual pads and a large resist window surrounding many pads may have to be employed.



2.7 DUMMY BOARD

Recommended dummy board size is 10 mm X and 10 mm Y outer of panel. For internal dummy, 3 mm is preferred with 2.4 mm spacing if the breakaway requires routing process both for horizontal and vertical internal dummies.



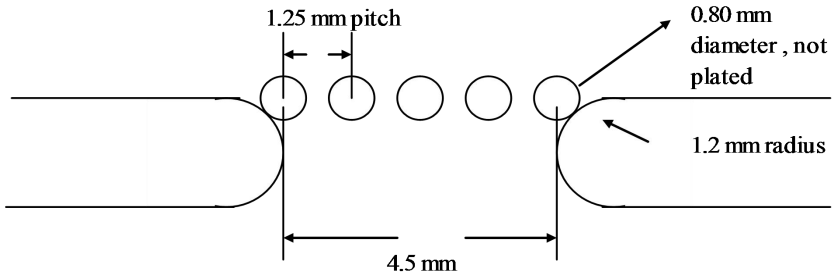
2.8 BREAKAWAY TABS

2.8.1 Mouse Bite

This type of breakaway is applicable for the following board application;

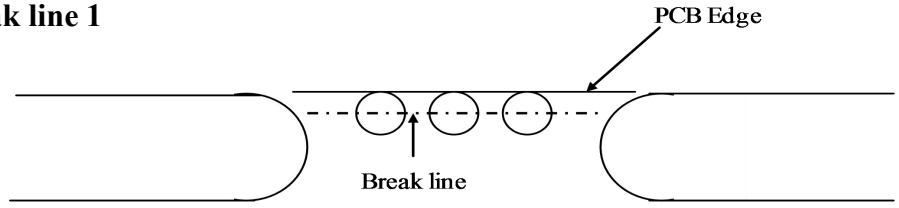
1. Irregular PCB design that requires radius or circular contour.
2. For PCB assembly that has flip chip, BGA, CSP and sensitive components that susceptible to cracking.
3. Components that are near the board edge.

Preferred design mouse bite design.



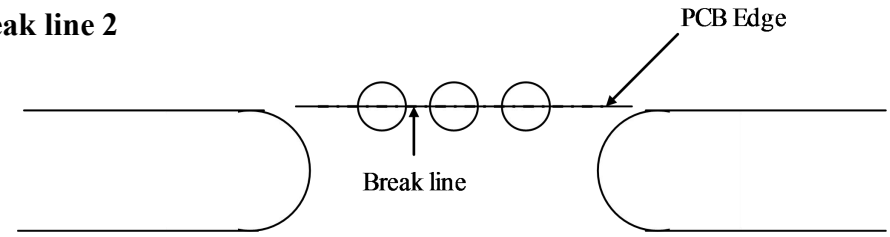
2.8.2 Types of Break Line.

Break line 1



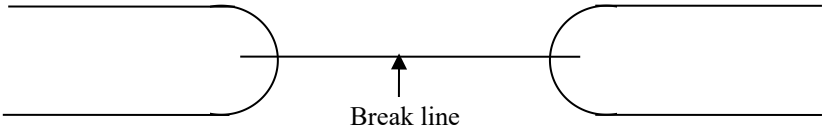
Suggested Application:
a. Board that has inner layer adjacent to the edge
b. Board that has no available space to accommodate the holes

Break line 2



Suggested Application:
a. Board that has no inner layer adjacent to the edge.
b. Availability of space for the holes

Break Line 3

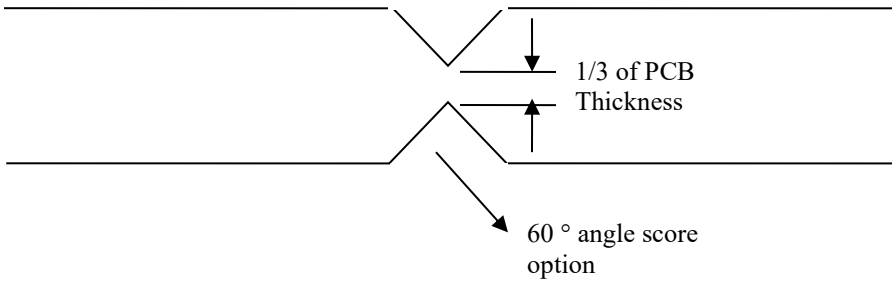


Suggested Application:
a. Board that has limited area to accommodate the holes
b. Board that has limited length to accommodate 1 to 3 holes with 1.25 mm pitch (mouse bite).

2.9 V-GROOVE

This type of breakaway is applicable for the following board application;
1. Rectangular and square board design.
2. No components near the edge of the board.
3. No components that is delicate to cracking during singulation.
4. Board that has 1 mm component distance from the edge.

Recommended V-groove standard design.



2.10 COMPONENT LEGEND

Whatever decision is made regarding the amount of legend used, the requirement for a separate, clear, pad ident drawing for component positions and orientations is still essential. Where screen printed idents are required the following points must be considered

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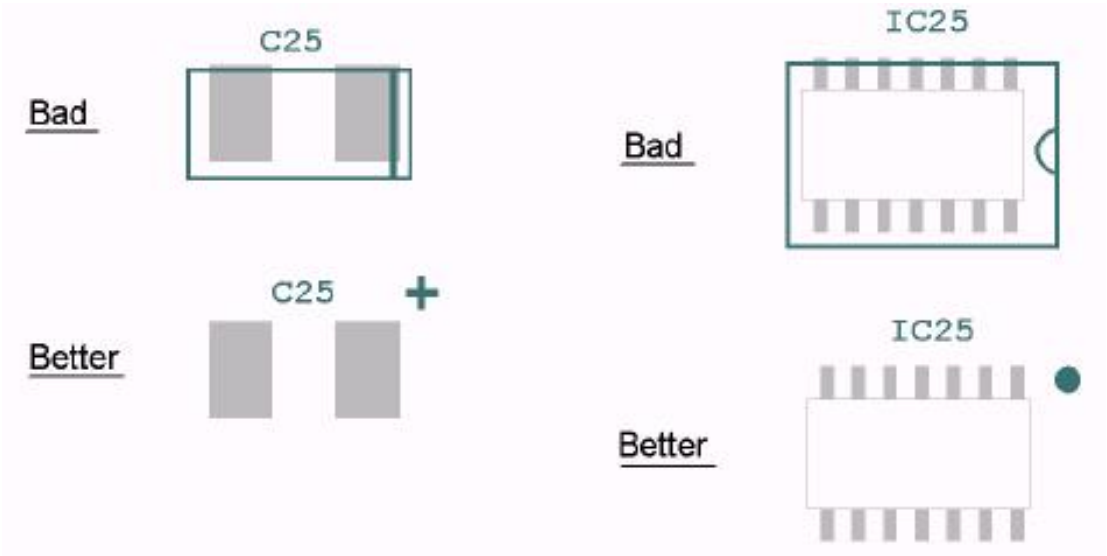
- The silk-screened layer should be designed such that it does not encroach onto components holes/pads. Recommended minimum distance between edge of silk screen and resist window edge is 0.5 mm (0.020 in.)----------0.25mm for ERF.
- Legends/circuit references should not be located directly underneath component positions where they may be obscured.
- Wherever possible the legend should be placed so that it may be read in two directions only top and bottom and left to right. Relevant orientation and polarity markings should be used where component orientation is critical.



SECTION 3: PAD DESIGN & LAND PATTERN

3.1 PAD DESIGN & LAND PATTERN

Pls. refer to IPC-7351 for the recommended Pad design/Land Patterns. This standard was based on industry component specifications, board manufacturing and component placement accuracy capabilities. These land patterns are restricted to a specific component, and have an identifying IPC-7351 land pattern name.

Three land pattern geometry variations are supplied for each of the device families; maximum land protrusion (Density Level A), median land protrusion (Density Level B) and minimum land protrusion (Density Level C).

Density Level A: Maximum (Most) Land Protrusion – For low-density product applications, the 'maximum' land pattern condition has been developed to accommodate wave or flow solder of leadless chip devices and leaded gull-wing devices. The geometry furnished for these devices, as well as inward and ''J''-formed lead contact device families, may provide a wider process window for reflow solder processes as well.

Density Level B: Median (Nominal) Land Protrusion – Products with a moderate level of component density may consider adapting the 'median' land pattern geometry. The median land patterns furnished for all device families will provide a robust solder attachment condition for reflow solder processes and should provide a condition suitable for wave or reflow soldering of leadless chip and leaded gull-wing type devices.

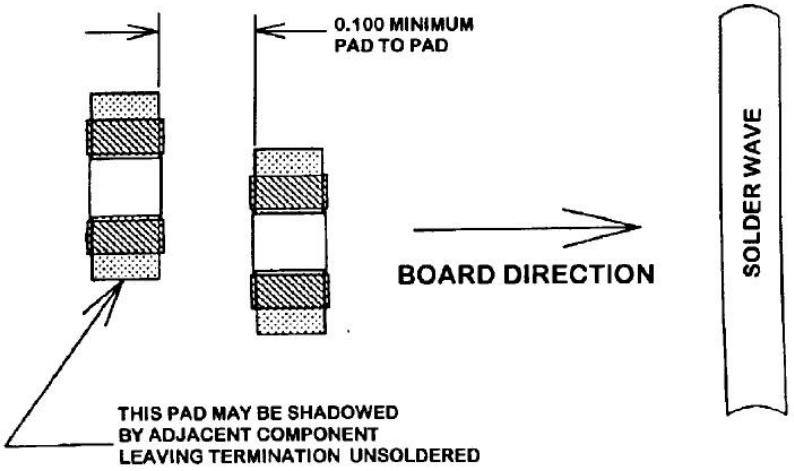
Density Level C: Minimum (Least) Land Protrusion – High component density typical of portable and hand-held product applications may consider the 'minimum' land pattern geometry variation. Selection of the minimum land pattern geometry may not be suitable for all product use categories. Although all three land pattern geometry variations are considered compliant for lead free soldering processes, the Density Level C variant will require more processing capability to ensure a proper wetting of the lead free alloy. It is important to note, however, that the primary issue of lead free relates to the surface finish on the printed board and the component termination.

SECTION 4: COMPONENT PLACEMENT & ORIENTATION

4.1 COMPONENT SPACING

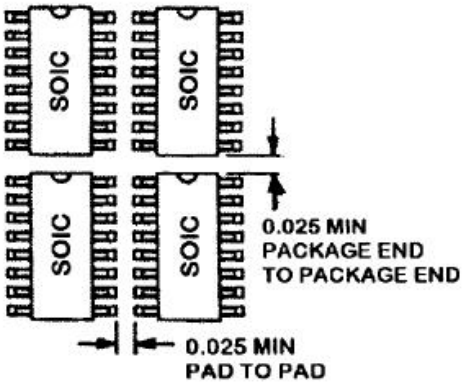
Component to component spacing is critical to soldering, rework, test and automated assembly. If components are placed too close together, the placement head of pick and place machines may interfere with other components requiring manual placement of some parts. Also, any of these conditions may cause a longer more costly assembly process and less reliable product.

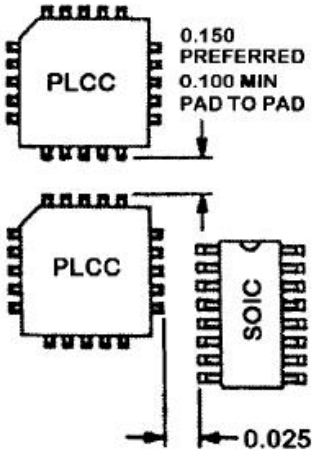
When placing chip components on the bottom of a board in a staggered pattern, a minimum spacing of 0.100" is required to insure that shadowing and unsoldered terminations do not occur (see Figure 5-2).



MINIMUM DISTANCE REQUIRED BETWEEN STAGGERED CHIP COMPONENTS WHEN WAVE SOLDERING

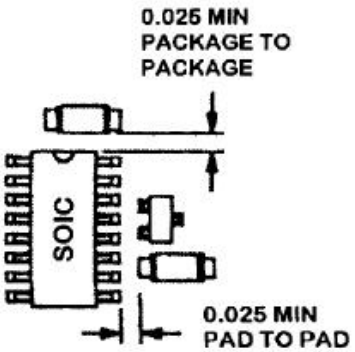
Minimum component spacing for the most common package types are shown in Figures 5-3 and 5-4. Care should be taken when designing with new or non-standard parts to provide the clearance required for assembly, rework and test. Generally the component to component spacing will be 1X the component height (preferred) or 1/2 the component height (minimum). Manufacturing engineering or the assembly vendor should be consulted when questions of spacing arise. A component to component spacing equal to the height of the package should be used when designing whit large components (over 0.20" high) such as SMT sockets, inductors and tantalum capacitors. This allows enough room for visual inspection and rework of solder joints.

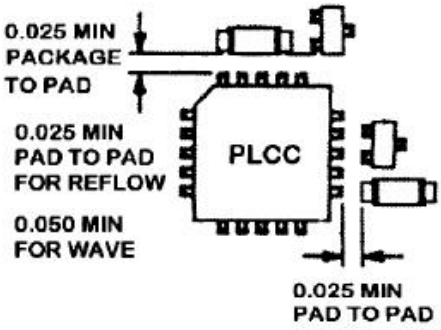


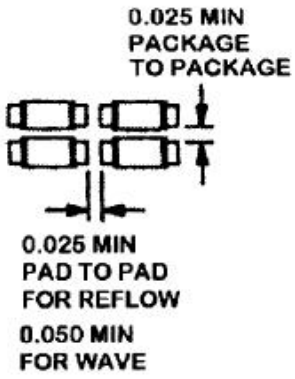


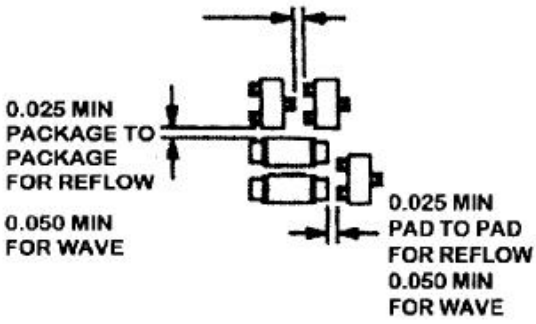
0.050 for ERF

0.050 for ERF









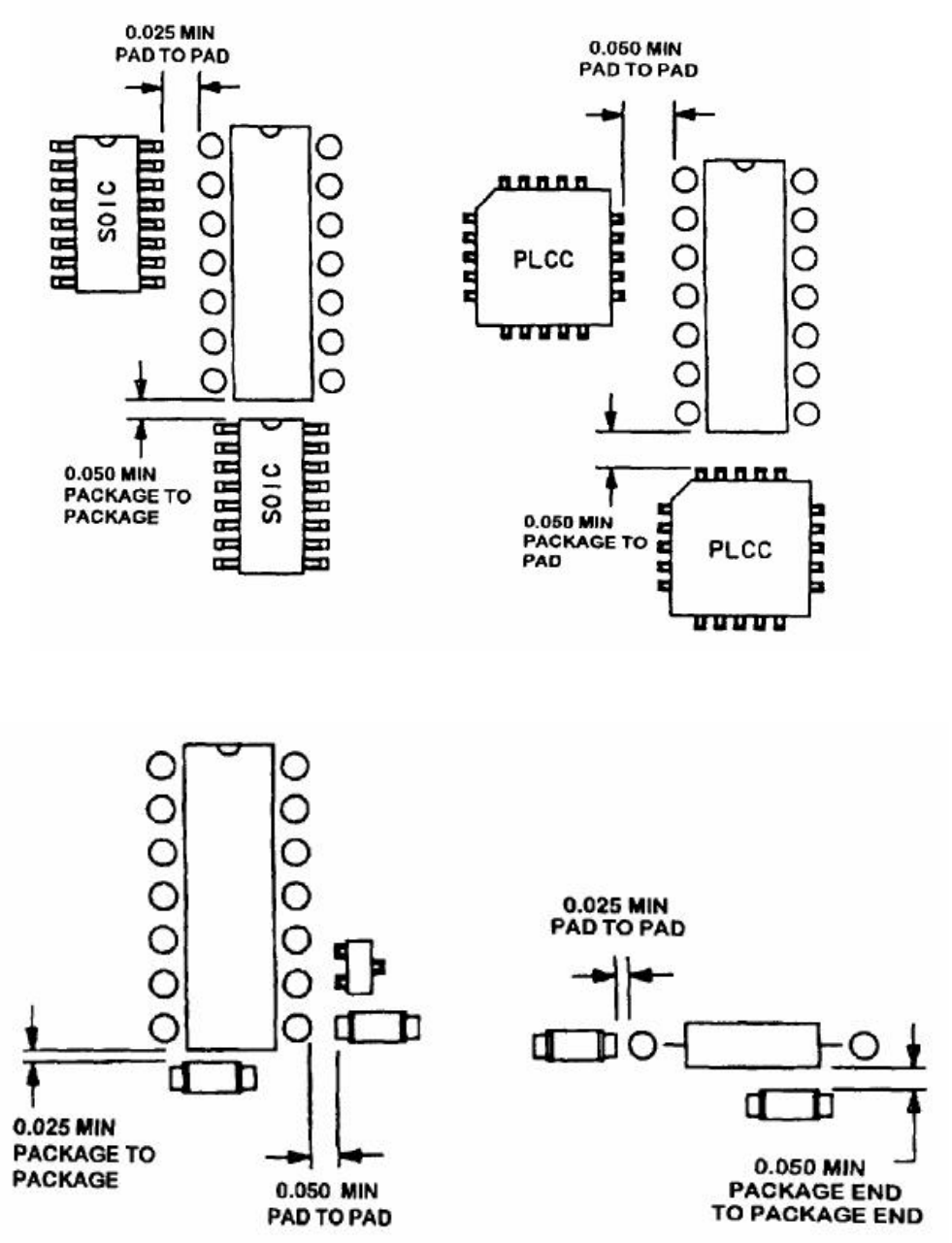
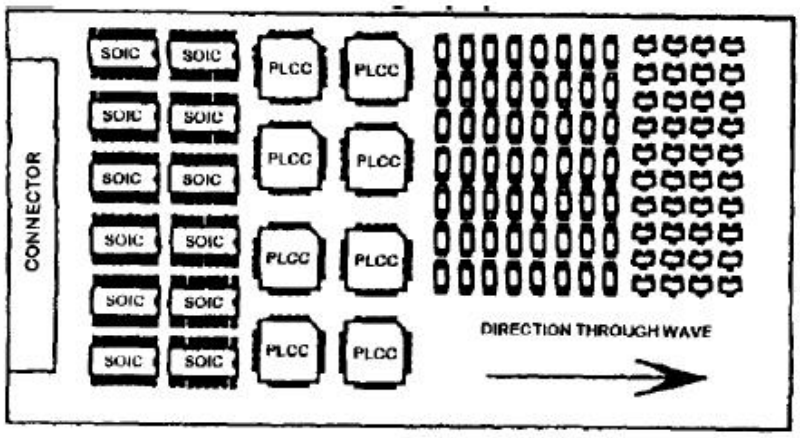


Figure 5-3 SMT TO THRU-PIN COMPONENT SPACING

4.2 COMPONENT AND BOARD ORIENTATION

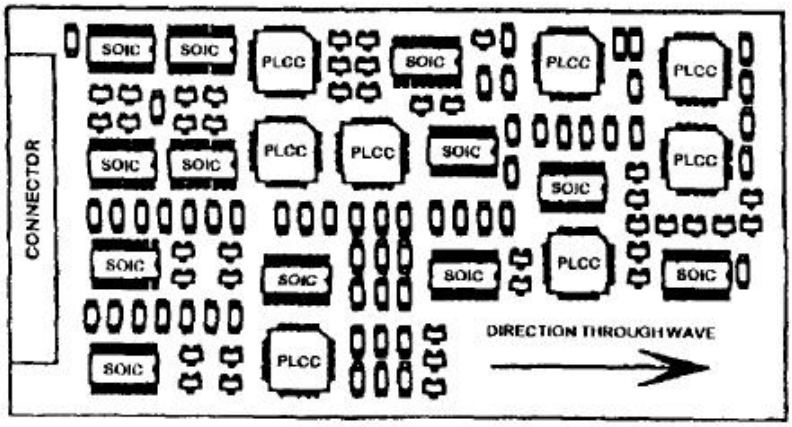
Component orientation has a direct effect on the quality and reliability of reflow and wave soldered

assemblies. Poor unreliable solder joints, unsoldered connections and tombstoning of components are some results of incorrect placement and orientation. The size and geometry of the board outline, tooling holes, the location of connectors and components at the edge of a board will determine the direction of flow through placement and soldering equipment.



WHEN THE LARGE COMPONENTS ARE BUNCHED UP AS IN THIS DESIGN THE BOARD WILL HAVE TO BE REFLOWED AT HIGHER TEMPERATURES THAN NECESSARY AND DAMAGE TO CHIP COMPONENTS MAY OCCUR.

NON-PREFERRED COMPONENT PLACEMENT



BY SPREADING OUT THE LARGE COMPONENTS EVENLY OVER THE DESIGN, BETTER THERMAL DISTRIBUTION IS ACHIEVED FOR SOLDERING

PLACEMENT FOR THERMAL DISTRIBUTION

A component to component spacing equal to the height of the package should be used when designing with large components (over 0.20" high) such as SMT sockets, inductors and tantalum capacitors. This allows enough room for visual inspection and rework of solder joints.

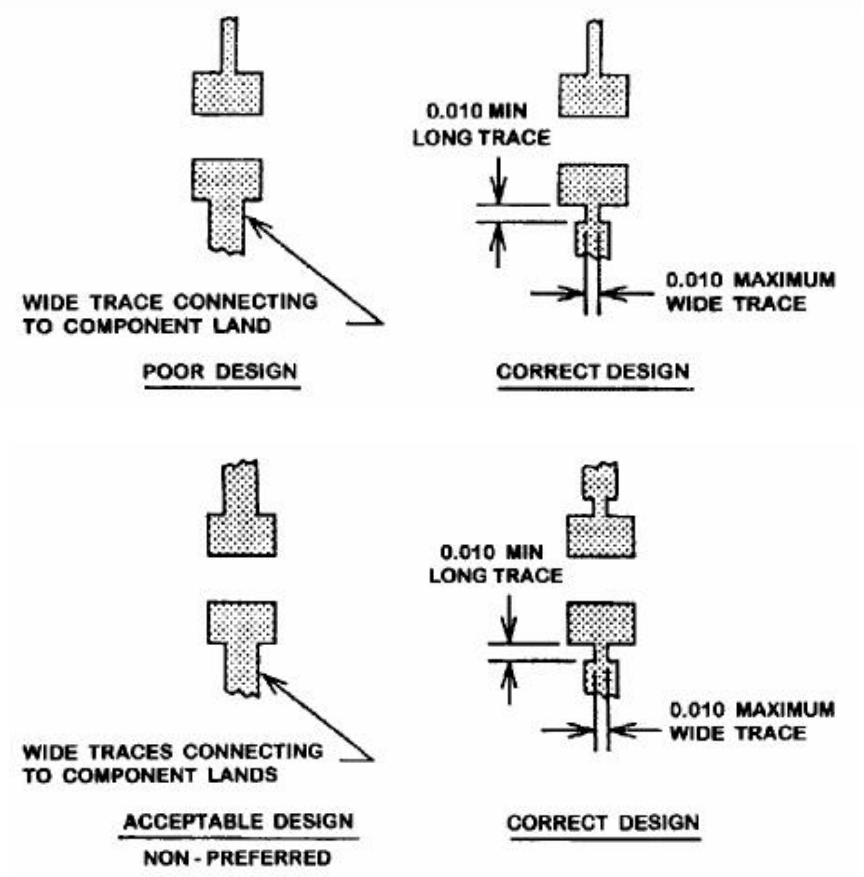
Thermal considerations require that the component density be distributed about the available board space as evenly as possible and concentrations of large components be avoided. When components are spread out over the board, one area of the board will not be substantially hotter than another during reflow (see illustration above). Even component distribution is also required to aid in balancing the routing across the surfaces and layers of the board and to minimize bow and twist. (See Section 5 for balanced routing requirements.)

SECTION 5: TRACE ROUTING & PLATING

5.1 TRACE ROUTING TO COMPONENT LANDS

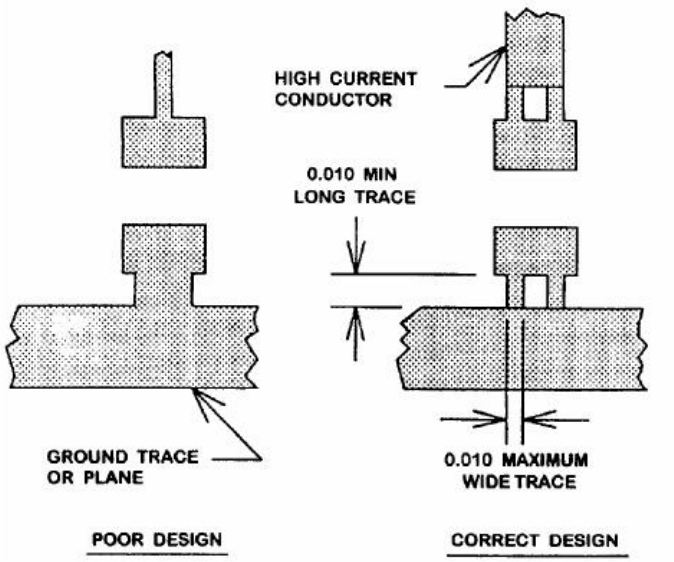
Large traces connecting to a component land may cause heat to migrate away from the component termination resulting in poor solder joints. In cases where solder mask is not used, solder may flow

away from the component termination causing an open solder joint. Necking the trace down as it enters the land prevents the solder and heat from migrating away from the pad and helps to thermally balance the land pattern. The trace should be a maximum of 0.010" wide connecting to the pad and a minimum of 0.010" long from the pad to a large trace as shown below. If the circuit design requires a wide trace to be connected to component lands, the traces connecting both lands should be the same width and the smallest possible dimension.



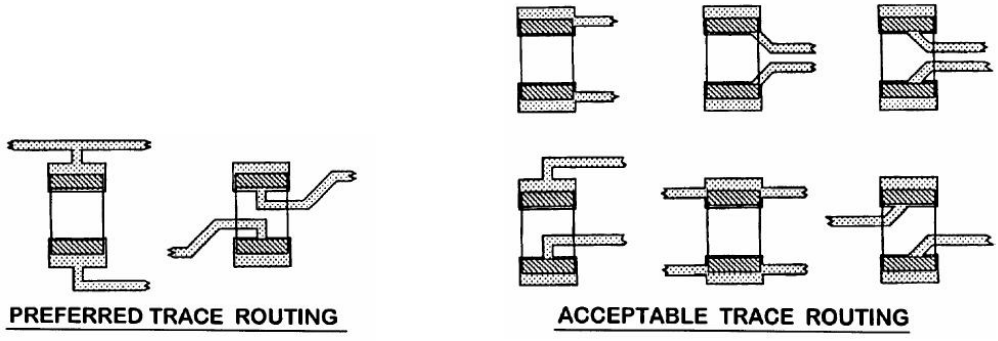
CONNECTING THICK TRACES TO COMPONENT LANDS

When connecting component pads to large ground traces, or wide high current conductors, the traces must be necked down and balanced to prevent the migration of heat (and solder if solder mask is not used) to large conductor areas. More than one trace may be used to connect ground planes and large traces to land patterns. The traces should be a maximum of 0.010" wide connecting to the pad and a minimum of 0.010" long from pad to large trace or plane (see illustration below).



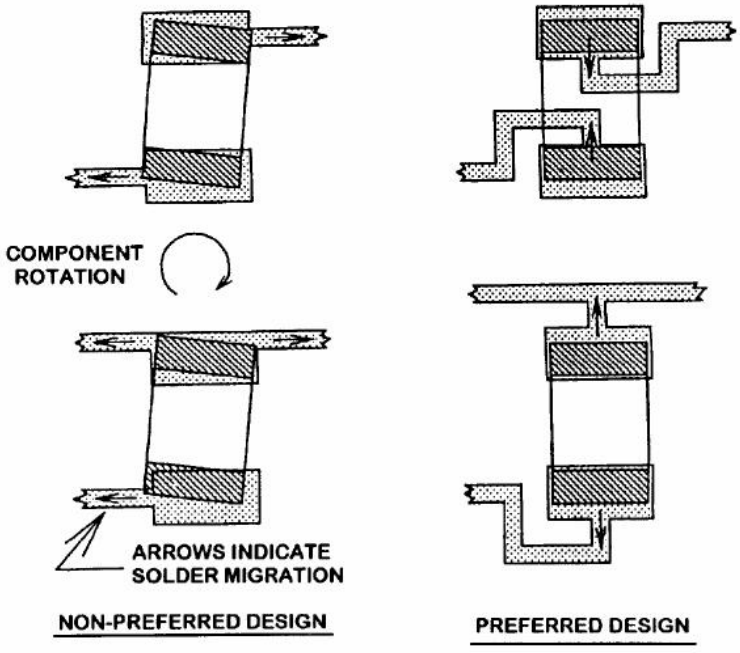
CONNECTING COMPONENT LANDS TO LARGE CONDUCTORS

Signal traces should connect to component pads using one trace per pad, preferably connecting to the outside or inside edges of the pads in a symmetrical manner. When using solder mask on the board, the angle and location of the connecting traces are not as critical as non-solder masked designs. Generally any routing which keeps the amount of trace connecting the component pads balanced will be acceptable. See Figure below for an example of trace routing.



CONNECTING TRACES TO COMPONENT LANDS WHEN USING SOLDERMASK

When routing traces to chip component pads and solder mask is not used on the board, it becomes critical to route the connections in such a way to keep the solder from migrating away from the pad and pulling the component out of alignment. Traces should be routed to both inside or outside edges of the pad to keep the solder tension evenly distributed on both terminations of the component. Illustration below shows the preferred method of connecting traces to chip pads.



CONNECTING TRACES TO COMPONENT LANDS WHEN SOLDER MASK IS NOT USED

5.2 VIA ROUTING GUIDELINES

Test via spacing will be 0.100" preferred, 0.050" acceptable.

Do not place vias under axial through hole components as the component may be damaged during soldering when solder flows up through the via hole.

Do not place vias in a location where it would be possible to insert a component incorrectly. For example: 0.100" away from each end of a sip package.

The placing of vias under chip components on wave soldered assemblies is not recommended, as solder flowing up through the via may lift or break the component, or possibly short a component to pad. If the chip component is located on the solder side of the board, avoid placing vias under or near the component where it may interfere with areas used to epoxy the component to the board (see Illustration below).

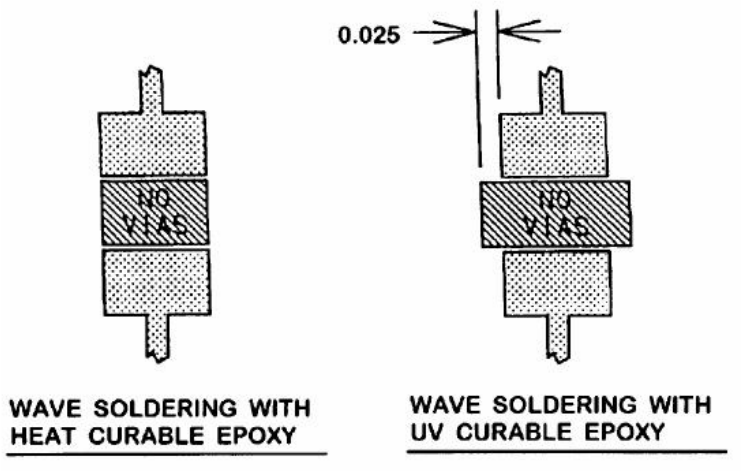
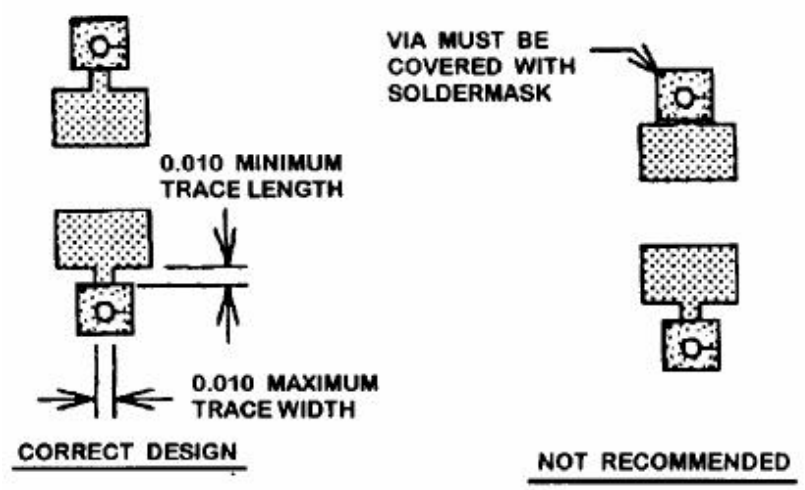


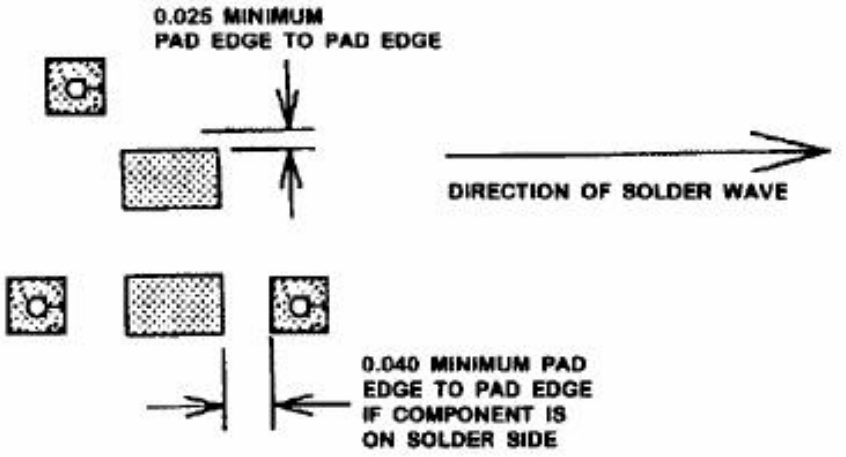
Figure 6-5 VIA PLACEMENT FOR SOLDER SIDE CHIPS

Vias connecting to a component pad shall have a minimum clearance of 0.010" from via edge to component land edge and maximum trace width of 0.010" (see Illustration below). Spacing under 0.010" are not recommended but may be useful on extra dense designs. If vias are to be placed closer than 0.010" to a component pad, they must be covered with solder mask.



CONNECTING VIAS TO COMPONENT PADS

Vias not connecting to component pads will have a minimum clearance of 0.025". When the PCB is to be wave soldered, via clearance to component pads on the solder side of the PCB will be 0.040" if the via is placed before or after the pad in the direction of solder wave (see Illustration below).



VIA TO COMPONENT PAD SPACING

5.3 PLATING

Recommended plating:

a. Hot Air Solder Level (HASL) – applicable for simple SDM components (chip components) with non-fine pitch IC.
b. Electroless Nickel/Gold – applicable for fine pitch components, BGA, Flip Chip, CSP, COB and lead free.
c. Chemical Tin Lead – applicable for fine pitch IC (QFP) using tin lead finish.
d. Organic Solder Protection (OSP) – Alternative for lead free application (cheaper than Electroless.